The EMU DCOPS alignment readout system (rev by D. Eartly)

Status of 10.12.00

E. Orischin, V. Sknar

Introduction

Choice of the link protocol is directly associated with an architecture of the readout system. As a base of the system architecture we consider suggestion of Jorge Moromisato (see attachment: **Architec.pdf**, Fig. 1.). It can be taken as final with one note: ADC and DSP should not be arranged at the node in outer ring. Reasons are the following:

1. The CCDs require three control signals with the pulse rise/fall time not more than 50 ns (typically 10 ns). To satisfy this condition all control signals must be buffered.
2. To transmit the CCD output analog signals through a long cable without distortion it is necessary to convert them into current.

Thus, we are to use additional components that increase power assumption and cost without winning in quality. We suppose that the front-end processor is to be arranged near the sensor board, and ADC should accomplish it.

Then we can talk about dividing of the readout board into two parts: the front-end part with ADC and DSP part (with interface), to move DSP to a periphery of the detector. But we have several objects requiring a control in the front-end part: DAC, ADC, digital thermometer, voltage regulators, and timer. So we are to provide individual interfaces to them. Such link between two parts is too complicated to be right.

System architecture

Thus, considering suggestion of Jorge Moromisato as a base, we suggest the structure of the alignment readout system shown in Fig. 2. (Fig. 1 belongs to the file **Architec.pdf**. To exclude confusion, the figure numbers begin from 2). Fig. 3 –5 are the exemplars to the system architecture.

The alignment readout system contains the host computer equipped by two standard RS-485 multiplexers; each of them serves one endcap. Each channel of the multiplexer (i.e. port) is connected to six interface boards arranged on a periphery of the chamber layer.

The interface board shown in Fig. 6 performs two functions: RS-485/LVDS conversion and low voltage distribution. The interface board serves one radial LVDS link providing control and readout of five SLM sensors, one Transfer Line (TL) sensor.

Using of LVDS inside of the chamber layer provides the low producing noise link, low power assumption and low cost. RS-485 is used for outer links to provide the reliable link for a long distance.

Data exchange protocol

An investigation of existing protocols showed that none of them could be applied for the alignment readout system. This result coincides to opinion of another group (HV monitoring). Details can be discussed later. Our suggestion is the following.

Each readout board has its physical address defined by switches or connector. It is necessary to avoid wrong addressing when one of the readout boards is failed.
Any command contains an address. All readout boards compare this address with their physical addresses, and perform received command if address is in coincidence. Address can be individual or group in dependence on a type of operation.

The RS-485/LVDS interface boards do not have own addresses; that is they are transparent. Each channel of the multiplexer is the port of the host computer. Thus, full address of the readout board consists of the port address and the readout board address, and the address field of one port can be arranged into one byte.

Only one readout board can be accessible for reading at any time. The read data are directed from the selected board to the host without passing through other boards.

Consideration of some parts

Low Voltage Distribution
The existing scheme of the low voltage distribution in the radial link should stay. It includes one +12 V line and DC-DC converters arranged at each readout board.

Voltage Regulators
Two approaches exist to solve the problem of the magnetic field effect: using of the air core inductors or trek to the inductorless voltage regulator. Unfortunately, market of the air core inductors does not have values more than 2.2 uH. Therefore we have prepared tooling for manufacturing of inductors.
Final decision will be accepted later.

Front End Processor (Correlated Double Sampler)
There are integrated front-end processors oriented to the CCD, such as AD9803, AD9807 and similar ones from another manufacturers (Hitachi and so on). All of them have two disadvantages: a large power assumption (about 100 mA) and high cost, because they are oriented to the color CCD and therefore contain parts, which are unnecessary for our application.
Thus, Correlated Double Sampler (CDS) should stay without sizable change.

DSP and Flash Memory
One of the problems associated with the DSP and flash memory is the radiation tolerance. Only Texas Instruments provides the military program for DSP among other manufacturers. But the class S (Space) DSP are extremely expensive (up to $500 per chip). ADSP-2185L (or ADSP-2187L) stays as the most suitable DSP for our application.
Our aim is not to decrease probability of the DSP failure, but to provide its reliable work in any conditions. We see the only way to solve this problem: possibility to download code into flash memory and to initialize DSP. It means that the downloading must be performed without participation of the DSP.

Interface
The most painful malfunction is 'hanging' of the transmitter that can occur as a result of DSP failure. To avoid this we suggest to include the hardware timeout circuitry, which disconnect the line driver from a line. Then failed board will cannot affect to others. Status of the board can be checked; and the program code can be redownloaded into the flash memory.

Structure of the DCOPS readout board is shown in Fig. 7.

Design problems

3. Arrangement of the readout boards.
   As it was mentioned above the readout board should be arranged near the detector board. It is necessary to define acceptable dimensions and an arrangement of the fastening holes.

4. Data development.
   Is algorithm of the data development defined now?

5. Length of cables.
   How far is the counting room from detector?
   This is especially important for an arrangement of the power supplies.

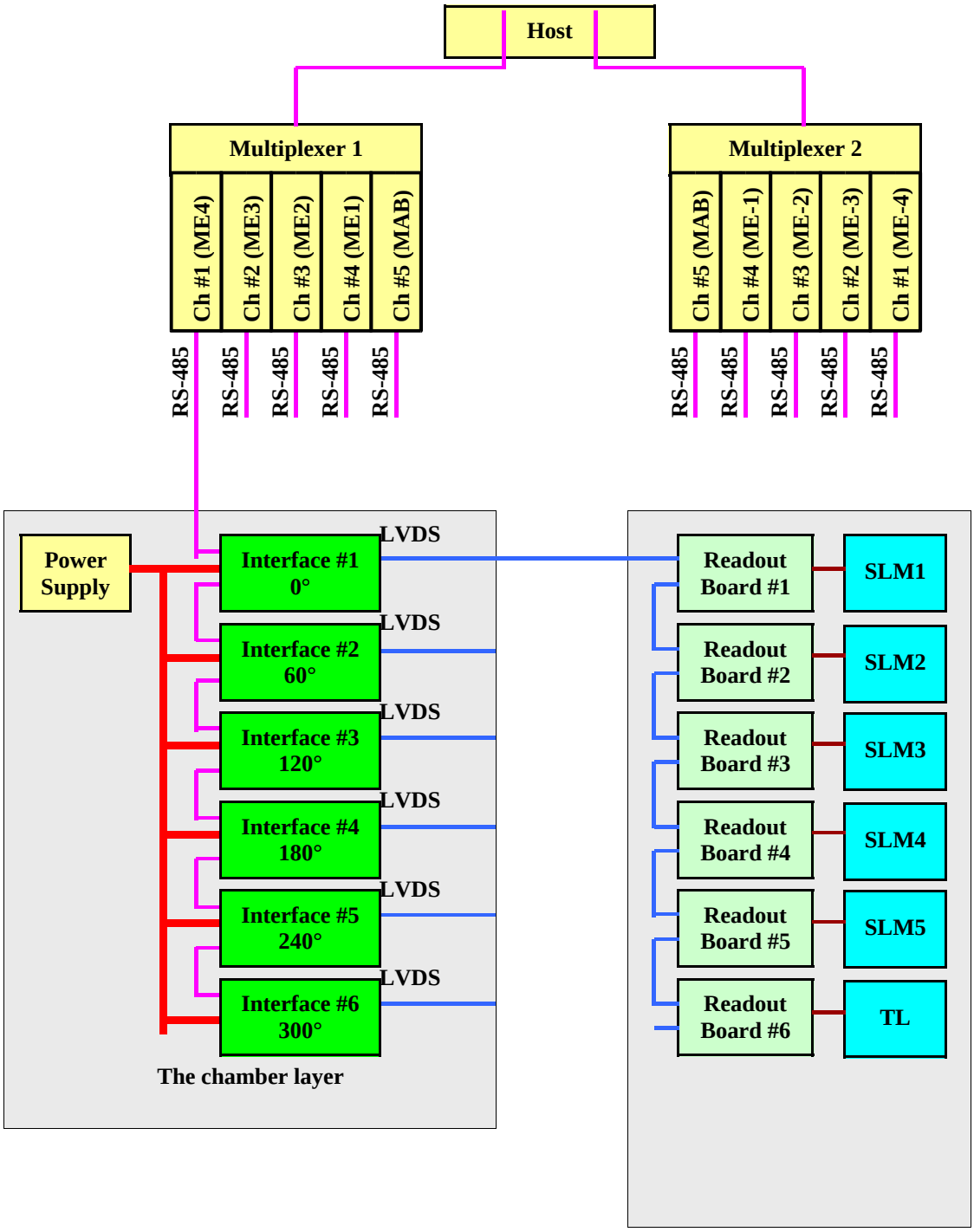

Fig. 2. The EMU DCOPS Alignment Readout Architecture

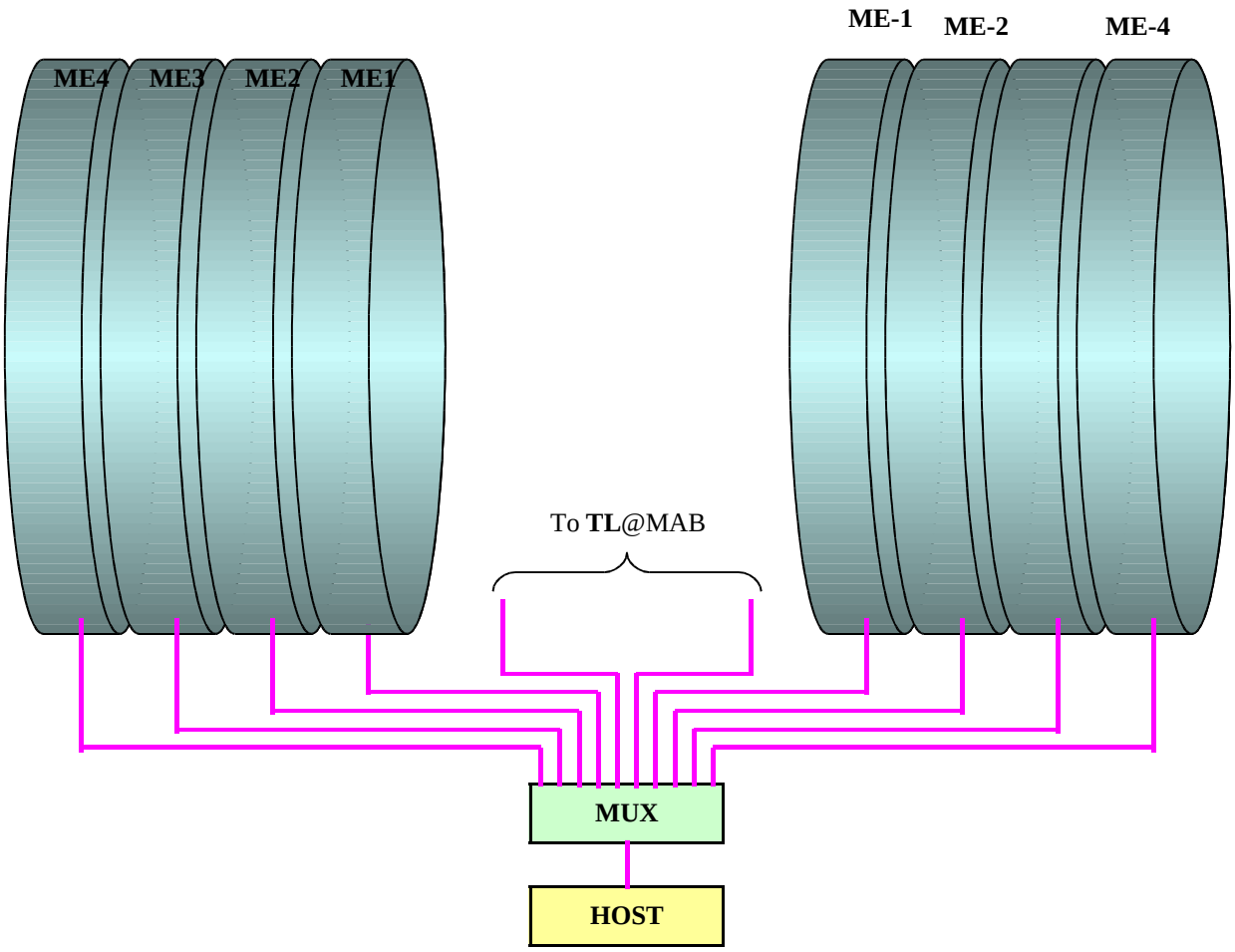

Fig.3. Linking with the host

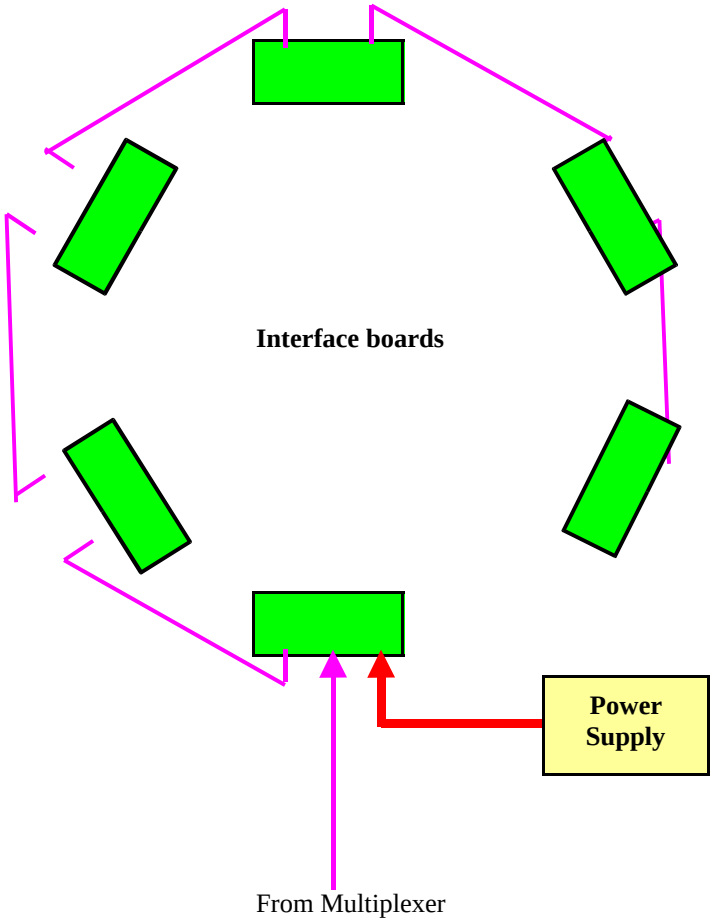

Fig.4. Linking and power distribution for the chamber layer

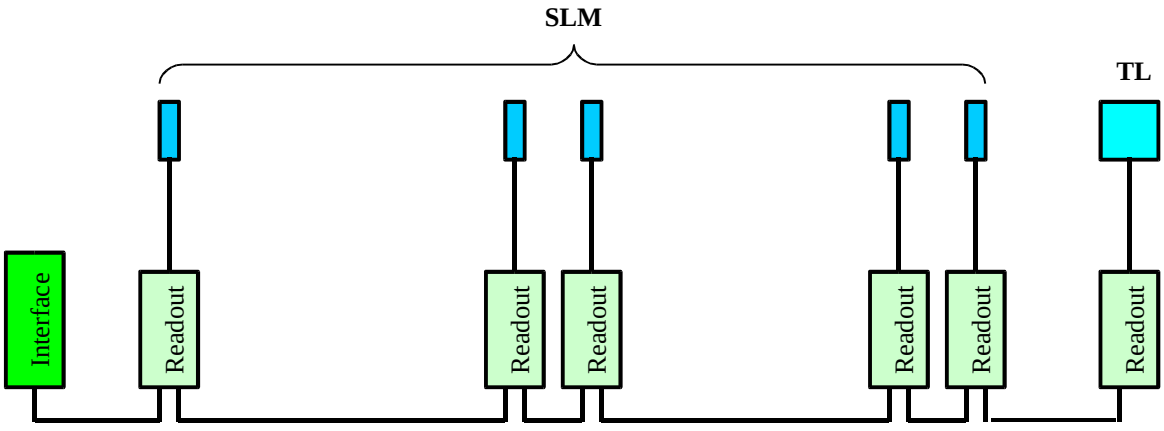

Fig.5. The radial readout structure

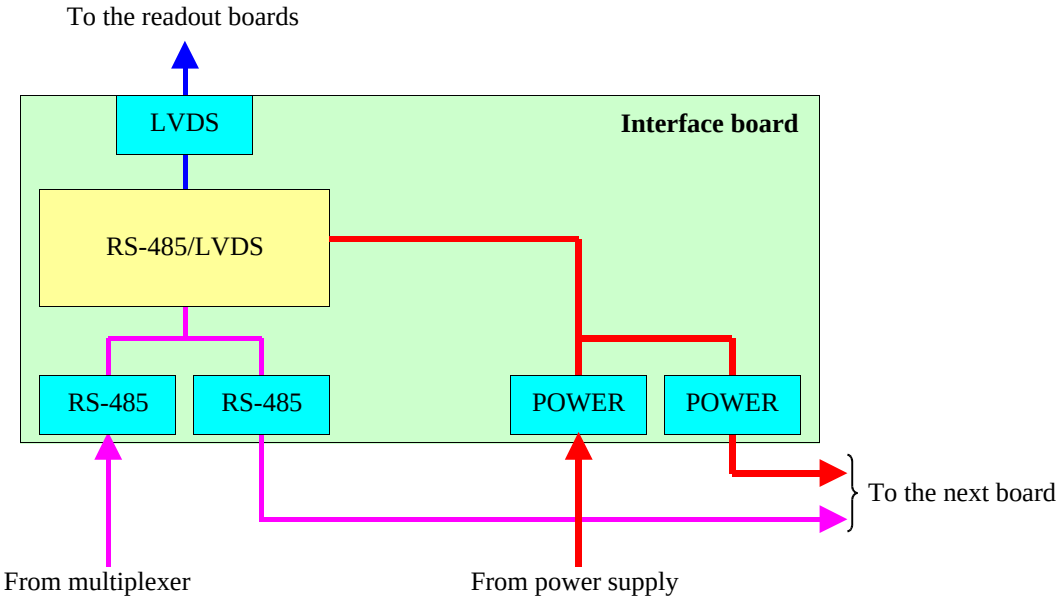

Fig.6. Structure of the interface board

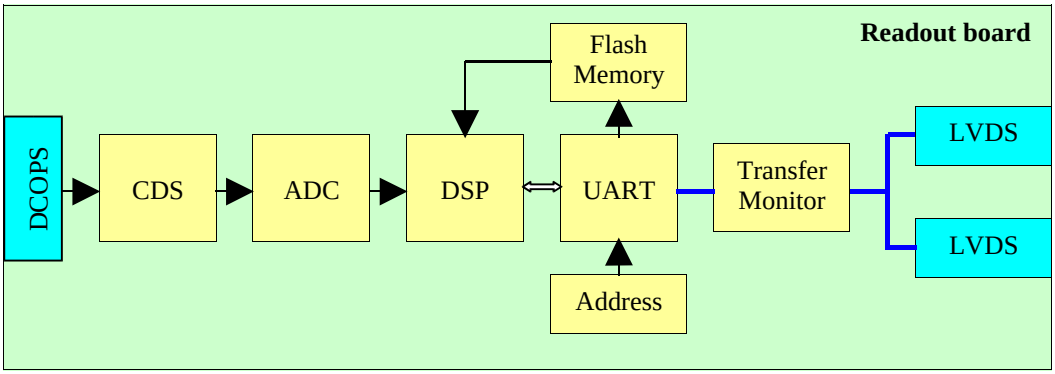

Fig.7. Structure of the readout board